UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,683	04/20/2001	Robert L. Shuler JR.	MSC-22953-3	5289

24957 7590 05/03/2005

NASA JOHNSON SPACE CENTER
MAIL CODE HA
2101 NASA RD 1
HOUSTON, TX 77058

EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/840,683	SHULER, ROBERT L.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *18 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,10-16 and 22-37* is/are pending in the application.

4a) Of the above claim(s) *14-16 and 22-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,10-13 and 30-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/18/05 has been entered.

Specification

2. The disclosure is objected to because of the following informalities: on page 11, FET "612" in the comparison chart is objected to because Figure 6 shows "612" for a circuit, not a transistor. Appropriate correction is required.

Claim Objections

3. Claims 31-33 are objected to because of the following informalities:

In claim 31, line 4, it appears that "of the first channel" should be deleted because it only makes sense if adjusting the characteristic of an FET (not type of the channel, i.e., n-channel or p-channel).

In claim 32, line 2, it appears that "of the first channel" for the similar reason as in claim 1, i.e., it only makes sense to change the width/length of the transistor (not the channel).

In claim 33, it appears that "first channel" should be changed to --first FET-- for the similar reason as discussed.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 11-13 and 30-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 11, the phrase "wherein said two or more logic elements further comprising a plurality of logic gates ... fan out" is indefinite because the recitation "said two or more logic elements further comprises a plurality of logic gates" is confused since the two or more logic elements are separated elements so the combined elements (two or more logic elements) comprises the plurality of logic gates renders the claim indefinite since it is not clear whether each of two or more logic elements comprise a logic gate or more than a logic gates. Further, "the plurality of logic gates and the two or more logic elements" on line 3 in the above phrase also renders the claim indefinite because it appears that the plurality of logic gates are different from the two or more logic elements which contradicts to the recitation recited earlier that the two or more logic elements comprises the plurality of logic gates (i.e., if the two or more logic elements comprises the plurality of logic gates, then why it is recited "the plurality of logic elements and the two or more logic elements"). Further "the slowest of the plurality of logic gates" on line 5 lacks antecedent basis and it appears that it should be changed to —- slowest logic gate of the plurality of logic gates--. Clarification and/or appropriate correction is requested.

Claims 12 and 13 are indefinite because of the "plurality of logic gates and each of the two or more logic elements" is indefinite for the similar reasons as in claim11, and also because they include the indefiniteness of claim 11. Further, in claim 12, "without being reduced in size" on line 5 render the claim indefinite because it is not clear which is not reduced in size; if the output pulse response is not reduced in size then it also would contradict to the recitation recited earlier that the glitch is prevent from passing through since it is too small (i.e., if the glitch is not passing through then there is no such output pulse response then how can it be "without being reduced in size". Clarification and/or appropriate correction is requested.

With respect to claim 34, "inserting a non-linearity into the first channel" is indefinite because it is not understood "non-linearity" of what, and "non-linearity" by itself is not a physical element so it is not clear how can it be inserted into a channel. Clarification and/or appropriate correction is requested. Also, "first channel" on line 2 appears that it should be changed to --first FET-- for it to make sense.

Claim 35 is indefinite because it includes the indefiniteness of claim 34. Further, "non-linearity" on line 1 is also indefinite for the similar reason as in claim 34.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 8, 10, 11, 30-33, 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bansal (USP 5,504,703).

With respect to claim 8, Figure 3 of the Bansal reference discloses a latch circuit, which includes: a logic gate (T1, T2) having an input (node 4) and an output (node 1); and a feedback path (path goes from node 1 to node 4) from the output (node 1) to the input (node 4) of the logic gate, wherein the feedback path includes two or more delay elements (INV1, INV2, INV3, INV4); wherein the logic gate and the two or mode delay elements each comprising an input to output pulse response (input-to-output signal) operable for delaying a propagation time of a pulse propagating therethrough and for selectively reducing a pulse width therefore (due to the delay propagate therethrough and the delay of the rise time and fall time of the logic gate/element that the signal is propagated therethrough); and the logic gate and the two or more logic elements being operable for reducing in size an instance of a potentially SEU producing glitch introduce at the input of the logic gate before the potential SEU producing glitch propagates through the feedback path to the input of the logic gate (i.e., configured to absorb a glitch at the input of the logic gate before it propagates through the feedback path to the input of the logic gate, Col. 3, lines 28-36 and 52-64). The Bansal reference does not disclose that each of the inverters (T1-T2, INV1, INV2, INV2, INV4, T3-T4) has a same delay. However, it is known in the art that the two CMOS inverters that have the same size (i.e., the PMOS of the first inverter having the same size as the PMOS of the second inverter, and the NMOS of the first inverter having the same size as the NMOS of the second inverter) will have the same time-delay. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 3 of the Bansal reference by making the size of each PMOS transistor of the inverters (T1-T2, INV1, INV2, INV2, INV4, T3-T4) equals to each other, and the size of each NMOS transistor of the inverters (T1-T2, INV1, INV2, INV2, INV4, T3-T4) equals to each

other for the purpose of easily design the circuitry and the fabrication process is simple. Thus, this modification will meets all the limitations of this claim because each of the inverters has the same delay, so the input to output pulse response of the logic gate and the two or more logic elements being substantially similar in that the resulting amount of pulse propagation delay and amount of reducing of the pulse width of the potential SEU producing glitch is spread substantially evenly among the logic gate and the two or more logic elements (i.e., the delay being spread evenly among the logic gate and the inverters in the feedback path).

Note with claim 10, as discussed in claim 8 above, because every element in the latch is an inverter, and because each of the inverters in Figure 3 of Bansal having the same size (all PMOS transistors having the same size, and all NMOS transistors having the same size), so the rise time and fall time of each inverter in the latch must be the same, and thus the limitation of claim 10 is met.

Insofar as understood in claim 11, the two or more logic elements in Figure 3 of Bansal including a plurality of logic gates (INV1-INV4), and it is inherent that the input to output pulse response of each of the inverters INV1-INV4 being configured to produce a pulse propagation delay (every inverter must have a propagation delay) approximately no longer than a maximum pulse propagation delay of a slowest logic gate of the plurality of logic gates when the slowest logic gate is fully loaded with maximum fan out (i.e., when an inverter is loaded with a maximum fan out so it must have a maximum delay, and because each of the inverters in Figure 3 of Bansal is modified to have the same size so each of the inverters has the same delay, and clearly the delay cannot be longer than the maximum delay).

With respect to claims 30 and 37, the modification of the circuit in Figure 3 of Bansal as discussed above with regard to the rejection of claim 8 meets all the limitations of these claims as the modification circuitry including one more logic gates (T1-T2, T3-T4), and the one or more logic elements (INV1-INV4). Note that, regarding to the limitation of pulse width L1 and pulse width L2, these limitations are met in the operation of the circuitry because each logic element in the circuit must have a same delay (as discussed in claim 8 above), and if a glitch having a pulse width that is too small (i.e., less than a predetermined threshold pulse width, say L1) then the glitch cannot pass through a respective of the one or more logic gates and/or a respective of the one or more logic elements because such pulse width of the glitch is too small to trigger a logic device/circuit; and if the glitch has a pulse width greater than the predetermined threshold pulse width (L1) and less than a certain pulse width L2 (i.e., the pulse width is large enough to be affected by the delay of the logic device/circuit) then the glitch will pass through the respective of the one or more logic elements and of the one or more logic gates because the pulse width of the glitch is long enough to trigger the logic device/circuit and the output pulse width of the glitch then has a reduce pulse width (due to the rise time and fall time of the respective logic device/circuit). Note that because the delay of each of the inverters in the modification circuitry of Figure 3 has the same delay as discussed in claim 8 above, so the pulse width L1 is approximately equal for the respective of the one of more logic elements and for the respective of the one or more logic gates, and the pulse width L2 is also approximately equal for the respective of the one of more logic elements and for the respective of the one or more logic gates. Also, the circuit in Figure 3 is a latch circuit (claim 37).

Insofar as understood in claims 31-33 and 36, the modification as discussed above with regard to the rejection of claim 30 meets all the limitations of these claims except for adjusting the characteristic of the first FET which also includes making the first width and/or length wider/larger. However, it is old and well-known in the art that the delay of an inverter depends on the sizes of the transistors in the inverter (i.e., depend on the width and length of transistors). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the above modification circuitry by making the length and/or width of the transistors in each of the inverters (i.e., making the size of the transistors in each inverter larger/wider) in the modification circuitry of Figure 3 of Bansal for the purpose of achieve a specific desire delay. Thus this modification meets all the limitations of claims 31-33 that the characteristic of the first FET is adjusted and the adjusting comprising making the width and/or length of the transistor wider/larger. Note that, in claim 36, regarding to the limitation of pulse width L3, the limitations in this claim is met in the operation of the modification circuitry because when an input signal pulse having a pulse width that is too large (i.e., larger than a specific pulse width, say L3, i.e., the pulse width is large enough so that the input to output pulse response of the inverter is not affected by the delay of the inverter) then the input signal pulse will pass through the respective of the one or more logic elements and of the one or more logic without a substantial change in a resulting output signal pulse width (because the pulse width is too large compares to the rise time and fall time of the delay, so the affection of the rise and fall time to the output pulse is negligible).

8. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bansal (USP 5,504,703) in view of Weste et al ("Principle of CMOS VLSI Design: A System Perspective", 2nd edition).

Insofar as understood in claims 34 and 35, the modification as discussed in claim 31 above meets all the limitations of these claims except for the step of adjusting including making the first transistor having a non-linearity shape (which comprises a right angle). However, the Weste et al. reference discloses that one way of creating a larger size inverter is by changing the transistor shape (see Figure 5.7c) in which the transistor including a non-linearity shape (includes right angle, see Figure 5.7c) for the purpose of reducing the drain capacitance (see lines 3-7, page 278). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the above modification circuitry (as discussed in claim 31) by using the transistor shape as taught in Figure 5.7c of the Weste reference when making the transistors of each of the inverters larger for the purpose of reducing the drain capacitance and thus improving the performance of the circuitry. Thus, this modification meets all the limitations of claims 34 and 35 as the first FET including a non-linearity shape (includes a right angle).

Response to Arguments

9. Applicant's arguments filed on 3/18/05 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. In view of the significant indefiniteness problems noted above, the scope of claims 11 and 12 cannot be determined, no prior art can be applied against these claims at this time. This is not an indication of allowability to these claims.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 27, 2005

LONG NGUYEN
PRIMARY EXAMINER